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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,067	08/27/2003	Ruban Kanapathippillai	42P14037D2	4624

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EXAMINER	
CHANG, DANIEL D	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/649,067	KANAPATHIPPILLAI ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-24 and 40-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-24 and 40-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/8/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Acknowledgement

Receipt is acknowledged of the Amendment filed July 27, 2006 and IDS filed August 8, 2006.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 20-24 and 40-57 are rejected under 35 U.S.C. 102(b) as being anticipated by Watanabe (US 5,808,490).

Regarding claim 20, Watanabe discloses, in Figs. 2A and 3, a bus state keeper comprising:

a plurality (since bus control circuit 21 shown in Fig. 3 is provided in an LSI device and is for a bus in system, it is inherent and/or intended that there are more than one. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987)) of multiplexers (MUX 21c) each having

a select input (*0), a first input ("0" connected to OUT), a second input ("1" connected to output of latch 21b), and an output (output of 21c), the output coupled to each respective bit of

a first bus (22) coupled to a plurality of devices (23a-23c), wherein the first bus is to be kept in a steady state when inactive (col. 3, line 46 - col. 4, line 34; col. 5, lines 4-23),

the first input coupled to each respective bit of a second bus (OUT),

the select input of each of the plurality of multiplexers coupled to a select signal (*0); and

a plurality (again, since bus control circuit 21 shown in Fig. 3 is provided in an LSI device and is for a bus in system, it is inherent and/or intended that there are more than one. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987)) of flip flops (21b; see Fig. 7) each having a data input (D in Fig. 7), a data output (Q in Fig. 7) and a clock input (clock input *G), the data input coupled to each respective bit of the first bus (via $21a_1$ and IN),

the data output coupled respectively to the second input of the plurality of multiplexers, the clock input coupled to a clock signal (clock input *G),

the plurality of flip flops to store a state (see Tables 1 and 2) of the first bus in response to the select signal (col. 6, lines 59+).

Regarding claim 21, Watanabe discloses, in Figs. 2A and 3, that the plurality of flip flops are clocked by the clock signal (*G) to store a state of the first bus (col. 6, lines 59+).

Regarding claim 22, Watanabe discloses, in Figs. 2A and 3, that the select signal (*0) input to each select input of the plurality of multiplexers (21c) selects between outputting from

the plurality of multiplexers a stored state (output of 21b) in the flip flops onto the first bus (22) or

outputting the state of the second bus (OUT) onto the first bus (when OUT is selected by *0).

Regarding claim 23, Watanabe discloses, in Figs. 2A and 3, that the select signal input to each select input of the plurality of multiplexers (21c) selects to output from the plurality of multiplexers (21c) a stored state in the flip flops (21b) onto the first bus to maintain a state of the first bus (col. 3, line 46 - col. 4, line 34).

Regarding claim 24, Watanabe discloses, in Figs. 2A and 3, that the select signal maintains a state of the first bus (22) to conserve power (col. 4, lines 31+).

Claims 40, 41, and 43 are essentially the same in scope as apparatus claims 20-24 and are rejected similarly.

Regarding claim 42, Watanabe discloses, in Figs. 2A and 3, that wherein each of the plurality of flip flops are a single bit D type flip flop (see Fig. 7 and Table 1).

Regarding claim 44, Watanabe discloses, in Figs. 2A and 3, that wherein when the input bus (OUT) is selected (by *0) to be output by the plurality of multiplexers (21c), the bus state keeper drives the state of the input bus onto the output bus (22) to change the state of the output bus (col. 3, line 46 - col. 4, line 34).

Claims 45-52 are essentially the same in scope as apparatus claims 20-44 and are rejected similarly.

Regarding claims 53-57, since bus control circuit 21 shown in Fig. 3 or 4 is provided in an LSI device and is for a bus in system, it is intended that the one of the plurality of devices

23a-23c can be any of a flip flop or a memory block. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

Response to Arguments

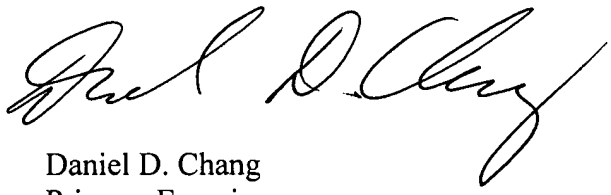
Applicant's arguments with respect to claims 20-24 and 40-57 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Daniel D. Chang
Primary Examiner
Art Unit 2819

dc